At the core of PA-RISC is an instruction set containing 140 carefully selected, fixed format instructions. Because the instruction set is simplified, instructions can be hard-wired directly into the CPU. Hard-wiring eliminates microcode and the necessity to decode complex instructions. This allows the processor to operate at maximum performance.

PA-RISC utilizes a load/store design and register-to-register operations to reduce the number of memory accesses. To further enhance performance, optimizing compilers schedule instructions and manage the instruction pipeline. With hard-wired control, a load/store design, and optimizing compilers, instructions can be executed on virtually every clock cycle. Single cycle instruction accounts for much of the superior performance of PA-RISC.

As one of the first major vendors to deliver a RISC-based system, Hewlett-Packard is one of the leading manufacturer of RISC-based computers today.

VLSI Technology Leadership
PA-RISC was designed to provide user benefits independent of the particular semiconductor technology implementation. HP's use of submicron CMOS Very Large Scale Integration (VLSI) technology allows the entire CPU to be integrated onto a single chip. The entire processor including the cache, Translation Lookaside Buffer (TLB) and floating point coprocessor are implemented on a single printed circuit board. Reduced complexity allows fewer components and higher reliability, and a resulting lower cost base.

Low Cost of Ownership / Small Footprint
Traditionally, business computers of this power have made use of liquid cooling. Mainframe vendors supplying older technology, CISC-based systems use hundreds of chips and components so closely packed that they are at risk of overheating unless liquid cooling is used. The HP 3000 Corporate Business System's advanced RISC-based VLSI allows use of CPU technologies that provide very high performance without the complexity that creates the need for liquid pumps and exorbitant tubing. This results in a system that has 1/12 the footprint of traditional mainframes, requires much less complex site preparation and maintenance, and is significantly less expensive to produce, own and operate.

Designed For Growth

The Corporate Business Systems were designed from inception to allow for future scalability and expandability. For example, the Corporate Business System 99X has a virtual address capability with an addressing range of 256 terabytes, allowing for substantial expandability to meet growing software requirements. In addition, the hardware architecture is designed to handle higher degrees of multiprocessing, including 8- and 16-way, and to capitalize on emerging technologies such as processor redundancy and fault tolerance.

Symmetric Multiprocessing
The HP 3000 Corporate Business System currently supports tightly coupled, symmetrical multiprocessing of up to four processors. Multiprocessing (MP) allows for economical, modular growth of processing power as system performance requirements increase, and performance capabilities will be augmented in the future with the introduction of higher degrees of multiprocessing in the CS 99X package. Multiprocessing in the MPE/iX software environment is entirely trans-